ABSTRACT OF THE DISCLOSURE

A design verification system utilizing programmable logic devices having varying numbers of logic processors, macro processors, memory processors and general purpose processors programmed therein is disclosed. These various processors can execute Boolean functions, macro operations, memory operations, and other computer instructions. This avoids either the need to implement logic or the need to compile the design into many gate-level Boolean logic operations for logic processors. Improved efficiency in the form of lower cost, lower power and/or higher speeds are the result when verifying certain types of designs.